ABSTRACT OF THE DISCLOSURE

PULSE-CONTROLLED MICROPIPELINE ARCHITECTURE

A control circuit for permitting a two-phase data transfer protocol between stages in a micropipeline. In accordance with the teachings of the present invention, the control circuit includes a control element for generating a data transfer control signal that governs data transport through a level-sensitive latch within the micropipeline. The control circuit further includes a dual-pulse generator receiving the data transfer control signal at its input and providing its output to the control input of the level-sensitive latch. The dual pulse generator converts a rising edge of the data transfer control signal into a first data transfer pulse and a falling edge of the data transfer control signal into a second data transfer pulse such that the micropipeline transfers data during both the rising edge and the falling edge.